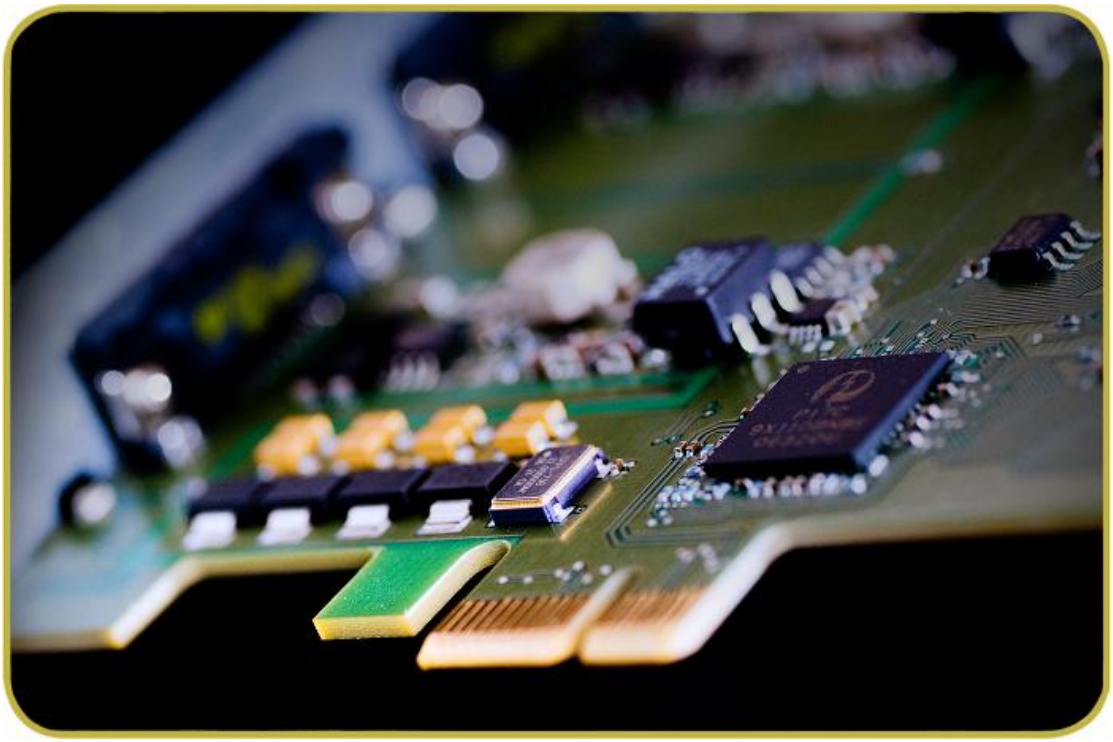
Kvaser PCIEcan User's Guide



Last updated Thursday, 22 April 2010

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1 Table of Contents

2 Introduction

2.1 Scope of this document

This document describes the following standard variants of the PCIEcan board:

Product Name	Item Number	Description
Kvaser PCIEcan HS	00425-2	One channel CAN interface
Kvaser PCIEcan HS/HS	00405-4	Two channel CAN interface

2.2 General Description

The Kvaser PCIEcan board connects up to two CAN networks to a PC using the PCI Express X1 bus. The Kvaser PCIEcan board is designed to fit the PCI Express bus systems and provides the user with excellent software support through Kvaser CANlib. Fully software compatible with the Kvaser PCIcan boards, i.e. 100% compatible with applications written for the Kvaser PCIcan boards using Kvaser CANlib API.

2.3 PCIEcan features

- Up to two independent CAN channels
- High Speed CAN
- Supports bit rates up to 1 Mbit/s
- Fits in PCI Express slots
- Communicates with the PC through Direct I/O
- Supports CAN 2.0 A and 2.0 B (active)
- DC/DC power supply to galvanically isolated bus drivers
- High-speed isolator circuits between CAN circuits and CAN drivers
- Fully software compatible with PCIcan and PCIcanx
- Quick and easy plug and play installation
- Extended temperature range of -40˚C - +85˚C
- Interfaces the CAN bus with DSUB connector(s)

3 Technical Specifications

The technical specifications for the PCIEcan boards are listed in Table 1and Table 2.

Table 1 Kvaser PCIEcan HS

General	
Size	PCI Express bus PC card, low profile, short length Approximately 56x121 mm (2.20x47.67 inc)
PCI card	Compliant with the PCI Express Bus Specification v1.0a
PCI bus interfaces	PCI Express slots
PCI Express bus size	X1 (fits in X1, X4, X8 and X16)
CAN bus connector	1 x 9-pin DSUB, male (See chapter 5.3)
Power consumption	PCIEcan HS: max 200 mA @ 3.3V.
CAN Controllers and Oscillator Frequency	
CAN controllers: 1 x SJA1000	
CAN Clock frequency: 16 MHz Option – Possible to specify CAN oscillator frequency per channel, contact our Sales Department for an inquiry.	
CAN Bus Driver(s)	
Drivers	Texas SN65HVD251D; compliant with the ISO 11898-2 standard.
Voltage feed	The drivers are galvanically separated from the power supply on the PC by on-board DC/DC converters.
Grounding	The ground of the CAN driver is available at the 9-pin DSUB connector.
Shielding	The shield of the CAN driver is available at the 9-pin DSUB connector.
Other Features	
• High-speed isolator circuits between CAN circuits and drivers. • Temperature range: -40˚C - +85˚C	

Table 2 Kvaser PCIEcan HS/HS

General	
Size	PCI Express bus PC card, low profile, short length Approximately 79x121 mm (3.09x47.67 inc)
PCI card	Compliant with the PCI Express Bus Specification v1.0a
PCI bus interfaces	PCI Express slots
PCI Express bus size	X1 (fits in X1, X4, X8 and X16)
CAN bus connector	2 x 9-pin DSUB, male (See chapter 5.3)
Power consumption	PCIEcan HS: max 300 mA @ 3.3V.
CAN Controllers and Oscillator Frequency	
CAN controllers: 2 x SJA1000	
CAN Clock frequency: 16 MHz Option – Possible to specify CAN oscillator frequency per channel, contact our Sales Department for an inquiry.	
CAN Bus Driver(s)	
Drivers	Texas SN65HVD251D; compliant with the ISO 11898-2 standard.
Voltage feed	The drivers are galvanically separated from the power supply on the PC by on-board DC/DC converters.
Grounding	The ground of the CAN driver is available at the 9-pin DSUB connector.
Shielding	The shield of the CAN driver is available at the 9-pin DSUB connector.
Other Features	
• High-speed isolator circuits between CAN circuits and drivers. • Temperature range: -40˚C - +85˚C	

4 Schematics

A block diagram for all product versions of the Kvaser PCIEcan boards is shown in Figure 1.

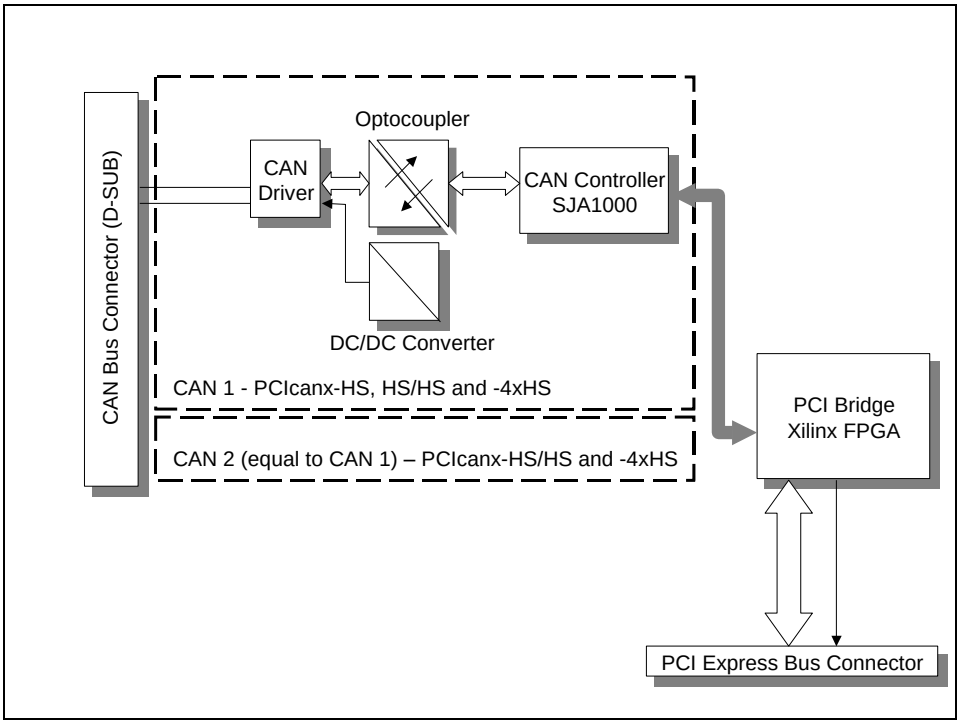

Figure 1 Block diagram for Kvaser PCIEcan -HS/HS.

5 The PCIEcan Hardware

For quick and easy installation, all Kvaser PCIEcan boards are plug-and-play boards.

5.1 The Isolated CAN Driver

KVASER's PCIEcan cards for CAN systems feature up to two CAN controllers. Each CAN-driver SN65HVD251D is isolated both from the CAN controller and all other CAN drivers. The CAN driver will get the necessary power from the PCI Express bus via an isolated DC/DC convert. The isolation between the CAN-controller and the CAN-driver has a delay of maximum 40 ns in each direction. This will reduce the possible cable length with 20 meter compared to having no isolation.

Due to human safety, the voltage should never at any part of the PCIEcan board be more than +/- 50 Volt from the PC-computer chassis ground. Note that the PCIEcan will not secure this condition itself. If any DSUB pin has an external voltage in the range below +/-500 Volt from chassis ground this will also be the true voltage at this pin.

Each CAN-driver circuit is protected from short time over voltage like ESD and accidental short cuts to high voltage. An over voltage beyond +/-500 Volt, on any used DSUB pin, will cause a rapid shortcut to ground. If the applied over voltage do have a high energy source some PCB wires may burn away in that case.

5.2 CAN Bus Termination

There are no terminating resistors onboard the standard PCIEcan board. However, there is room available to mount terminating resistors onboard all product versions. These terminating resistors can also serve as a load between the CAN bus wires; this is needed for the ISO 11898-2 compliant bus drivers to work properly. Please contact our Support Team for detailed instructions.

5.3 D-SUB connector

The D-SUB connector(s) are mounted on a bracket and connects to the metallic housing of the PC. The pinning of the 9-pin DSUB connector is listed in Table 3.

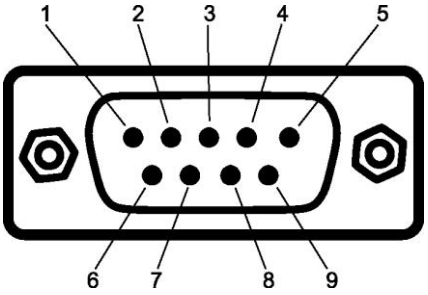

Table 3 9-pin DSUB connector for Kvaser PCIEcan HS, HS/HS. (Per channel)

Pin	Function
1	Not connected
2	CAN-L
3	Signal ground.
4	Not connected
5	Shield
6	Not connected
7	CAN-H
8	Not connected
9	Not connected

6 Software Development Information

This section is intended for those who want to program the PCIEcan card directly. Normally, you would choose to use the supporting device drivers available for the PCIEcan card. Refer to the “CANLIB Software Development Kit” documentation for further information on these device drivers from a programmer’s point of view. Please note that this board is fully software compatible with the Kvaser PCIEcan boards.

6.1 Additional Documentation

This document includes all information you need to use the circuits on the card. However, the circuits themselves are not described here so information about these must be obtained from the suppliers. See the list of references in chapter 8. General knowledge about the PCI Express bus is also assumed.

6.2 The PCI Express bus controller

All PCIEcan boards use the same PCI controller, which is an Xilinx FPGA with PCI core. The PCI controller is responsible for address decoding and interrupt steering.

The initialization of the PCI controller is outside the scope of this manual. Typically, it is carried out by the operating system and/or the BIOS. There are a few registers you have to set up in the driver; these are described below.

6.3 Address decoding

The PCI Express controller can decode up to 5 different address areas, three of which are used by the PCIEcan.

Address area #	Type	Size (bytes)	Used for
0	I/O	128	Xilinx registers.
1	I/O	128	SJA1000 circuits
			0 – 0x1f: SJA1000 #1
			0x20 – 0x3F: SJA1000 #2
			0x40 – 0x5F: SJA1000 #3
			0x60 – 0x7F: SJA1000 #4
2	I/O	8	Xilinx registers

Address area number 1, the one used for the SJA1000’s, is further subdivided into four areas of 32 bytes each; one for each (possible) SJA1000.

6.4 Interrupts

The PCIEcan uses one PCI Express bus interrupt, INTA#. It is asserted whenever one or more SJA1000's have their interrupts active. To reset an active interrupt, read the interrupt status register in all present SJA1000s – the interrupt of the corresponding SJA1000 will then automatically clear.

To check the status of the interrupt line, test the INTERRUPT ASSERTED bit (number 23) in the INTCSR register in the S5920.

To enable or disable interrupts from the PCIEcan, use the ADD-ON INTERRUPT PIN ENABLE (bit 13) in the INTCSR register in the S5920.

6.5 Registers in the Xilinx

The Xilinx FPGA implements a few registers.

Address offset	Register	Usage
0 – 6		Reserved, do not use
7	VERINT	Bit 7 - 4 contains the revision number of the FPGA configuration. 15 is the first revision, 14 is the next, and so on.

The current FPGA revision number is 10 (which is read from the VERINT register as 1110xxxx). Future revisions (9, 8, 7, …) will remain compatible with revision 10.

6.6 PCI Configuration Data

The following data are configured automatically into the Xilinx FPGA PCI controller when power is applied to the card.

Item	Value
Vendor Id	0x1A07
Device Id	0x0008
Revision Id	00
Class Code	0xffff00 (means: no base class code defined for device)
Subsystem Vendor Id	0x1A07
Subsystem Device Id	0x0008

6.7 Configuration of the SJA1000

Refer to the SJA1000 data sheet for all details on how to program the SJA1000. You need to know the following:

- RX1 is connected to ground.
- TX1 is not connected.
- CLKO is not connected.
- Setting the OCR register to 0xDA is a good idea. This means “normal output mode”, push-pull and the correct polarity.
- In the CDR register, you should set CBP to 1. You will probably also want to set the clock divider value to 0 (meaning divide-by-2), the Pelican bit, and the clock-off bit (you have no need for CLKOUT anyway.)

7 Support

The PCIEcan boards are supported by drivers routines and program examples for Windows 95/98/ME, Windows NT/2000/XP, Linux. The software and its documentation are available from our web site, and is not further documented here. Kvaser CANKing - a free-of-charge and general-purpose interactive CAN bus monitor can be download from our web site.

Please visit our homepage http://www.kvaser.com to find software updates, hints and tips and other helpful information. You are always welcome to contact our Support Team - support@kvaser.com.

8 References

Philips	SJA1000 Stand-Alone CAN Controller. Preliminary Specification. 1997 Nov 04. Also available on the web.
Shanley, T., and Anderson, D.	*PCI Express system architecture*. MindShare, Inc. ISBN 0-321-15630-7.

More CAN information is found on www.kvaser.com and has many links to other sites with CAN information. You can also download new versions of the software for PCIEcan here.

9 Legal Information

9.1 Electromagnetic compability

The equipment has been tested for compliance with the EN 50 081-2:1993 (emission) and the EN 50 082-2:1995 (immunity) standards.

9.2 RoHS directive

This product is manufactured in accordance with directive 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS.)

9.3 WEEE directive

This product is sold in compliance with the directive 2002/96/EC of the European Parliament on Waste Electrical and Electronic Equipment (WEEE.)

9.4 About this manual

We believe that the information contained herein was accurate in all respects at the time of printing. Kvaser AB cannot, however, assume any responsibility for errors or omissions in this text. Please also note that the information in this document is subject to change without notice and should not be construed as a commitment on the part of Kvaser AB.

9.5 Trademarks and patents

All product names mentioned in this manual are registered or unregistered trademarks of their respective owner.

The products described in this document are protected by U.S. patent 5,696,911.

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

10 Document revision history

Revision	Date	Changes
1	2008-01-17	Original revision
2	2008-12-01	Updated chapter 9 “Legal Information”